REMARKS

This Amendment seeks to place this application in condition for allowance. All of the Examiner's rejections have been addressed. Several of the pending claims have been amended. No new matter has been added.

OFFICE ACTION

In the office Action mailed August 1, 2000, the Examiner rejected claims 151-175 under 35 U.S.C. § 112, first paragraph, as containing subject matter not described in the specification in such a way as to enable one skilled in the art to which it pertains to make and/or use the invention. Furthermore, claims 166 and 172 were rejected as being so-called single means claims.

Finally, the Examiner determined that the instant application is not obvious in view of U.S. Patent 6,034,214 (hereinafter '214), the parent to the instant application. Should the Examiner change his position, Applicants would submit a terminal disclaimer to overcome such a rejection.

Rejection - 35 U.S.C. § 112:

Applicants respectfully disagree with the Examiner's rejection that the claims contain subject matter not described in the specification in such a way as to enable one skilled in the art to make and/or use the invention. Here, the Examiner stated that the specification does not provide support for the limitations directed to "providing first and second portions of a first amount of data

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synchronously with external clock signal transitions." Each rejection will be addressed separately below.

Claim 151

Claim 151 is directed to a method of controlling a memory device. The method requires, in part:

> issuing a write request to the memory device, wherein in response to the write request, the memory device samples first and second portions of data.

The specification on page 13, lines 13-17, page 20, lines 24-25, and page 21, lines 18-20, and Figures 2 and 3, describe and illustrate a master 11 (e.g., a CPU or bus controller) controlling a memory device 13. In a write operation, the master sends a write request to the memory device via the bus.

In response to the write request, the memory device samples and stores data from the master. In one embodiment, input receiver 71 (see, Figure 10) samples a first portion of the data at time 127 (see, Figure 13) and input receiver 72 (see, Figure 10) samples a second portion of the data at time 125 (see, Figure 13). In this regard, the specification on page 58, lines 18-21 states:

> The complement internal device clock is used to clock the 'even' input receivers to sample at time 127, while the true internal device clock is used to clock the 'odd' input receivers to sample at time 125.

Thus, the input receivers of the memory device sample first and second portions of the data.

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Claim 151 also requires:

> providing a first portion of data to the memory device synchronously with respect to a rising edge transition of an external clock signal; and
>
> providing a second portion of data to the memory device synchronously with respect to a falling edge transition of the external clock signal.

In one embodiment, the device interface of the master includes, among other things, an electrical interface which includes input/output circuitry, i.e., input receivers and bus drivers. (see, page 53, line 5-7). "A block diagram of the preferred input/output circuit ... is shown in Figure 10." (page 53, lines 24-25). In this embodiment, the input/output circuitry "consists of a set of input receivers 71, 72 and output driver 76." (page 54, lines 3-4).[1]

The output driver (76 in Figure 10) provides a first portion of the data to the memory device (via the bus) synchronously with respect to a falling edge of the complement internal device clock 74 (CLK\ of Figures 10 and 13) and provides a second portion of the data to the memory device synchronously with respect to a falling edge of the true internal device clock 73 (CLK of Figures 10 and 13). In this regard, the specification on page 58 lines 21-25 (emphasis added) states:

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[1] The specification at page 53, line 25 to page 54, line 8 states that (emphasis added):

> [The input/output] circuitry is particularly well-suited for use in DRAM devices but it can be used or modified by one skilled in the art for use in other devices connected to the bus of this invention. It consists of a set of input receivers 71, 72 and output driver 76 connected to input/output line 69 and pad 75 and circuitry to use the internal clock 73 and internal clock complement 74 to drive the input interface. The clocked input receivers take advantage of the synchronous nature of the bus.

> The true and complement internal device clocks are also used to select which data is driven to the output drivers. The gate delay between the internal device clock and output circuits driving the bus is slightly greater than the corresponding delay for the input circuits ....

Thus, the specification, as filed, describes that the output driver (76 in Figure 10) outputs data onto the bus synchronously with respect to falling edges of the true and complement internal device clocks (73 and 74 in Figures 10 and 13). A first portion of the data is output synchronously with respect to the falling edge of the complement internal device clock and a second portion of the data is output synchronously with respect to the falling edge of the true internal device clock.

In one embodiment, the true and complement internal device clocks are generated using an external clock and a delay lock loop circuit (see, page 57, lines 3-25).[2] The internal device clocks are synchronized with the rising and falling edges of the external clock. (see, page 58, line 1 to line 18 and Figure 13). Thus, in one embodiment, data is provided onto the bus synchronously with respect to a rising edge and a falling edge of the external clock, via output driver 76 and internal device clocks 73 and 74. (see, Figures 10 and 13 and page 58 lines 21-23 and page 53, line 25 to page 54, line 8).

In sum, Applicants submit that every feature of claim 151 is fully supported by the application as filed.

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[2] It should be noted that "[b]us clock information can be sent on one or two lines to provide a mechanism for each bused device to generate an internal device clock with zero skew relative to all the other device clocks." Specification, page 46, line 23 to page 47, line 1.

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Claim 158:.

Claim 158 also recites a method of controlling a memory device. Claim 158 recites, among other things:

> providing a first portion of data to the memory device synchronously with respect to a first external clock signal; and
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> providing a second portion of data to the memory device synchronously with respect to a second external clock signal.

As described above with respect to claim 151, the input receivers (see, Figure 10) sample data synchronously with respect to the falling edges of the internal device clocks 73 and 74 (see, Figures 10 and 13 and the specification at page 58, lines 18-21). Data is also provided onto the bus with respect to the falling edges of the internal device clocks 73 and 74. The sampling and outputting operations are described in the specification on page 58, lines 18-23:

> The complement internal device clock is used to clock the 'even' input receivers to sample at time 127, while the true internal device clock is used to clock the 'odd' input receivers to sample at time 125. The true and complement internal device clocks are also used to select which data is driven to the output drivers.

In one embodiment, the internal device clocks are generated by a delay lock loop using first and second external clocks 53 and 54 (see, Page 57, lines 3-25) to synchronize internal device clocks 73 and 74 with the external clocks 53 and 54 via delay adjustment of the internal device clocks 73 and 74. (see the time relationships illustrated by the dotted lines in Figure 13). Since the true and complement internal

device clocks are synchronized with the first and second external clocks, data is provided onto the bus synchronously with respect to the external clocks.

Applicants submit that every feature of claim 158 is fully supported by the application as filed.

Claim 166:

Claim 166 describes a memory controller for controlling a synchronous memory device. The controller includes:

> output driver circuitry to output data wherein:
>
> the output driver circuitry outputs a first portion of data in response to a rising edge transition of a first external clock signal; and
>
> the output driver circuitry outputs a second portion of data in response to a falling edge transition of the first external clock signal.

As mentioned above with respect to claim 151, the device interface of the master includes, among other things, an electrical interface which includes input/output circuitry. (see, page 53, line 5-7). In one embodiment, the input/output circuitry "consists of a set of input receivers 71, 72 and output driver 76." (page 54, lines 3-4, see also Figure 10).

The output driver (76 in Figure 10) outputs a first portion of the data synchronously with respect to a falling edge of the complement internal device clock 74 and outputs a second portion of the data synchronously with respect to a falling edge of the true internal device clock 73. In this regard, the specification on page 58, lines 18-23 states (emphasis added):

The complement internal device clock is used to clock the 'even' input receivers to sample at time 127, while the true internal device clock is used to clock the 'odd' input receivers to sample at time 125. The true and complement internal device clocks are also used to select which data is driven to the output drivers.

In one embodiment, the true and complement internal device clocks are generated using an external clock and a delay lock loop (see, page 57, lines 3-25).[3] The internal device clocks are synchronized with the rising and falling edges of the external clock. (see, page 58, line 1 to line 18 and Figure 13). Thus, in one embodiment, the output driver outputs data synchronously with respect to both rising and falling edges of the external clock, via output driver 76 and the falling edges of the internal device clocks 73 and 74. (see, Figures 10 and 13 and page 58 lines 21-23).

In sum, Applicants submit that every feature of claim 166 is fully supported by the application as filed.

[3] It should be noted that "[b]us clock information can be sent on one or two lines to provide a mechanism for each bused device to generate an internal device clock with zero skew relative to all the other device clocks." Specification, page 46, line 23 to page 47, line 1.

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Claim 172:

Claim 172 describes a memory controller for controlling a synchronous memory device. The controller includes:

output driver circuitry to output data wherein:
the output driver circuitry outputs a first portion of data in response to a first external clock signal; and
the output driver circuitry outputs a second portion of data in response to a second external clock signal.

As mentioned previously, the output driver (76 in Figure 10) outputs a first portion of the data onto the bus synchronously with respect to a falling edge of the complement internal device clock 74 (see, Figures 10 and 13) and outputs a second portion of the data onto the bus synchronously with respect to a falling edge of the true internal device clock 73 (see, Figures 10 and 13). In one embodiment, the true and complement internal device clocks are generated using first and second external clocks and delay lock loop circuitry (see, page 57, lines 3-25). In this embodiment, the delay lock loop circuit uses first and second external clocks 53 and 54 to synchronize internal device clocks 73 and 74 with the external clocks 53 and 54 via delay adjustment of the internal device clocks 73 and 74. (see, for example, the time relationship illustrated by the dotted lines in Figure 13). As such, the falling edges of the internal device clocks are synchronized with the edges of the external clocks. (see, page 58, line 1 to line 12). Thus, in this embodiment, output driver 76 output data in accordance with the falling edge of internal device clocks 73 and 74 which are in response to edge transitions of the external clocks. (see, Figures 10 and 13, page 57, line 3 to page 58, line 12, and page 58 lines 21-23).

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In sum, Applicants submit that every feature of claim 172 is fully supported by the application as filed.

Rejection - 35 U.S.C. § 112 over claims 166 and 172:

Applicants, to the extent understood, respectfully disagree with the Examiner's interpretation of claim 166 and 172 (i.e., a "so-called single means claims"). It is Applicants' position that 35 U.S.C. § 112, 6th paragraph, is not applicable to claims 166 and 172. In this regard, original and amended claims 166 and 172 do recite a means for performing a specified function. As such, 35 U.S.C. § 112, 6th paragraph is not pertinent.

In an effort to expeditiously advance the prosecution, however, Applicants have amended claims 166 and 172 to render the issue moot. Claims 166 and 172 have been amended to include "multiplexer circuitry, coupled to the output driver circuitry, to provide the first and second portions of data to the output driver circuitry." No new matter has been added.

CONCLUSION

Applicants request entry of the foregoing amendment prior to examination of this application. Applicants submit that all of the claims present patentable subject matter. Accordingly, Applicants respectfully request allowance of all of the claims.

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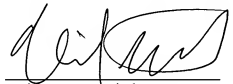
It is noted that should a telephone interview expedite the prosecution in any way, the Examiner is invited to contact Neil Steinberg at 650-944-7772.

Respectfully submitted,



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